EE 330
Homework 3
Spring 2024

Due: Friday Feb 2 at noon

Problem 1 Problem 1.6 of WH (WH refers to the Weste-Harris textbook) part b) only. Modify this problem to the design of this function first using the compound gate approach and second, using the static CMOS gate (NAND and NOR gates) approach. Compare the number of levels of logic and the total transistor count in the two approaches.

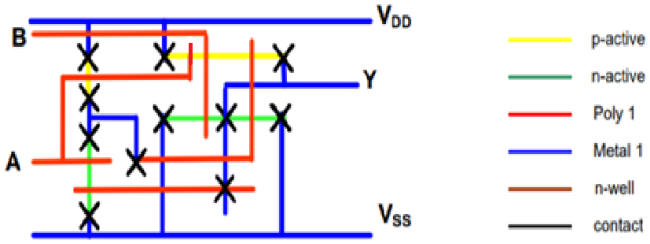
Problem 2 Problem 1.9 part a) only of WH. Restrict the gates you use in this solution to NAND gates only.

Problem 3 Determine the output transition time, t_{HL} if a two-input CMOS NOR gate is driving a 50fF load capacitance and both inputs transition from low to high at the same time. Assume all devices are minimum-sized and V_{DD}=5V.

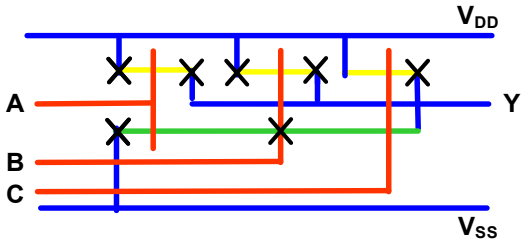
Problem 4 Give a transistor-level circuit schematic and sketch a stick diagram for a CMOS 3-input NOR gate designed by following a 3-input NOR gate with an inverter. The three inputs to the gate should be on the left side of the stick diagram and the output on the right side of the diagram. All inputs and the output should be in Metal 1.

Problem 5 Problem 1.15 of WH

Problem 6 The stick diagram of a circuit is shown. Give a circuit schematic for this circuit. The color-code for the stick diagram is shown to the right.



Problem 7 A stick diagram has been put together for a 3-input CMOS NAND gate and is shown below. There are one or more errors in this stick diagram. Identify and correct all errors in the stick diagram. The color-code for the stick diagram is shown in the previous problem.



Problem 8

Assume a CMOS inverter designed in the ON 0.18µ CMOS process drives 6 identical devices and the supply voltage is 2V. If a step input from 2V to 0V is applied at the input, what is the LH output transition time? Assume minimum-sized devices are used and also assume V_{DD}=2V.

Problem 9

A Metal-1 interconnect (shown in blue) is used to connect a VDD=2V supply voltage to a resistor with the ideal voltage across the resistor being 2V. Assume the nominal value of the resistor (shown in the purple box) is 50Ω. Unfortunately, there is some resistance in the interconnect, and this causes some voltage loss to the load when current is flowing through the interconnect. Assume the interconnect is made of aluminum and is 0.2um thick.

a) What voltage will actually appear across the 50 Ω resistor

b) What voltage would appear across the resistor if copper were used instead of aluminum for the interconnect. Assume it is of the same thickness.

c) The voltage drop can be decreased by increasing the width of the interconnect. How wide does an aluminum interconnect need to be to guarantee that the voltage drop across the load is no more than 5% below the supply voltage?

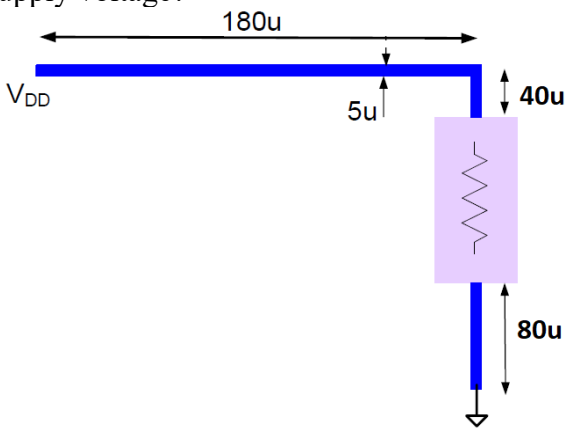


Figure 1: Problem 7

Conductivity of Al = 38 $S/\mu m$
Conductivity of Cu = 58 $S/\mu m$

Problem 10

Create in Verilog the following Boolean function. Use only the NOR gate you created in the last homework assignment. Create a test bench to test the Boolean function. Include screenshots of your Verilog code and simulation results.

$$F = \overline{A} \bullet B \bullet C + A \bullet B \bullet \overline{C}$$

(The + symbol denotes the Boolean "OR" operation and the • symbol denotes the Boolean "AND" operation. In future designations of Boolean operations, the " • " symbol will be suppressed, and the same function F will be designated as

$F = \overline{A}BC + AB\overline{C}$